Simulation Analysis of Hybrid Alternative Phase Apposition Disposition PWM Scheme for Cascaded Multilevel Inverters

N. Sujitha, S.Satish kumar, M.Sasikumar

Abstract— In this paper, we present the performance of a hybrid alternative phase opposition disposition pulse width modulation technique for soft switched cascaded five level inverters. The proposed modulation scheme inherits the switching loss reduction along with reduced harmonic performance of cascaded multilevel inverter fed drive system. The inverter topology used here has recently suggested in the area of high power medium voltage applications. The performance of this cascaded inverter has been analysed and compared with the results obtained from theory and simulation. Simulation study of the inverter employing the proposed HAPOD strategy has been done in MATLAB/SIMULINK.

Index Terms— Cascaded multilevel inverter, Hybrid alternative phase opposition disposition (HAPOD), Switching loss.

1 INTRODUCTION

Multilevel inverter has emerged recently in the area of high power medium voltage applications due to their advantages such as output waveform improvement which reduces the harmonic content in turn it reduces the size and cost of the filter and the level of electromagnetic interference (EMI) generated by switching operation. Multilevel inverters are of three types mainly; Diode clamped multilevel inverter, Flying capacitor multilevel inverter and Cascaded multilevel inverter. Among these three topologies cascaded multilevel inverters are most preferable since it overcomes the disadvantages of the other inverters. The main features of CMLI are

- 1. The level of extension is easy.
- 2. No voltage unbalancing problem.
- 3. It has modular structure.

New modulations are newly developed to generate a stepped switched waveform with high power quality and minimum switching frequency. In this paper we proposed a new hybrid alternative phase opposition disposition modulation scheme to produce an efficient output voltage.

2 SEQUENTIAL SWITCHING CASCADED FIVE LEVEL INVERTER

The proposed five level inverter consists of two hybrid cells with separate DC source. Each cell is made of full bridge inverter which has four sequential switching IGBT switches.

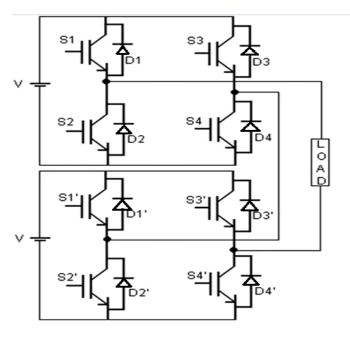


Fig. 1. Cascaded five level inverter topology

Proper sequential switching of inverter produces five level output voltages (2V, V, 0,-V,-2V). Sequential switching states of this proposed hybrid inverter is given in the below table.

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TABLE 1

SWITCHING STATE OF INVERTER

OUTPUT	S1	S2	S3	S4	S1`	S2`	S3`	S4`
VOLTAG								
Е								
2Vs	ON	OF	OF	ON	ON	OF	OF	ON
		F	F			F	F	
Vs	OF	ON	OF	ON	ON	OF	OF	ON
	F		F			F	F	
0	OF	ON	ON	OF	ON	OF	OF	ON
	F			F		F	F	
-Vs	OF	ON	ON	OF	ON	OF	ON	OF
	F			F		F		F
-2Vs	OF	ON	ON	OF	OF	ON	ON	OF
	F			F	F			F

(FPWM) and multiple sinusoidal modulation (MSPWM). The obtained output has both the features such as reduct

3 HYBRID MODULATION STRATEGY

3.1 Modulation scheme

The hybrid modulation meant in this paper is the combination of fundamental frequency modulation ion in switching loss from FPWM and good harmonic performance from MSPWM. This proposed hybrid modulation along with sequential switching and simple base PWM circulation scheme produces balanced power dissipation among the power modules. It consists of base generator, base PWM circulation module and hybrid modulation controller as shown in Fig. 2. The control parameters are fundamental frequency fo, carrier frequency fc and modulation index M=Am/KAc.

3.2 Base Modulation Design

Each cell needs three base modulation pulses and they are

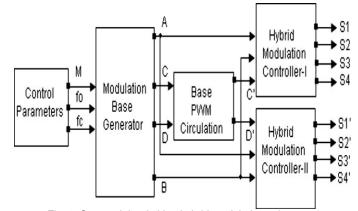


Fig. 2. Sequential switching hybrid modulation scheme

- Sequential switching pulse (SSP) denoted as 'A' which is a square wave pulse with half of fundamental frequency.
- 2) Fundamental modulation pulse (FPWM) is a square wave signal synchronized with the modulation signal is denoted by 'B'.
- 3) Multiple sinusoidal modulation pulse (MSPWM)-In this paper we used the alternative phase opposition disposition scheme. In APOD all the carriers are phase opposition by 180 degree from its adjacent carrier as shown in fig. 3.

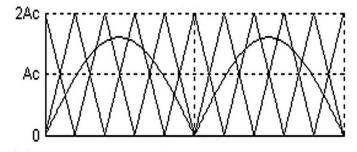
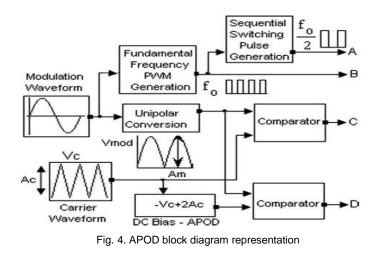


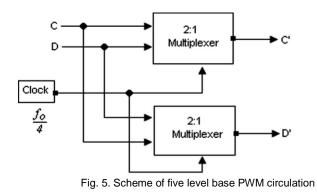
Fig. 3. APOD waveform

For cell 1 APOD signal 'c' is generated by comparing the unipolar modulation waveform with the carrier. For cell 2 APOD signal 'D' is obtained from comparison between the carrier with dc bias of –Vc+2Ac and unipolar modulation signal. The block diagram representation of APOD is shown in Fig. 4.



3.3 Base PWM Circulation

A simple base PWM circulation scheme is used to obtain hybrid PWM among the power modules. It consists of two 2:1 mux which select one of the two PWM signals based on the select clock signal. Clock frequency used here is fo/4 to circulate the PWM from one module to another. The order of the HPWM module is changed after each two fundamental frequency period (ie) first module becomes the second and the second module shifts to first. The five level base PWM circulation scheme is shown in Fig. 5.



3.4 Hybrid Modulation Controller

Sequential switching hybrid modulation pulses are generated by hybrid modulation controller by combining the SSP,FPWM and APOD signals. It is designed by a simple combination logic and it is expressed as,

S1 = ABC' + AB	and	S1' = ABD' + AB
$S2 = A\overline{B}C' + \overline{A}\overline{B}$		$S2' = A\overline{B}D' + \overline{A}\overline{B}$
$S3 = \overline{A} \overline{B}C' + A\overline{B}$		$S3' = \overline{A} \overline{B} D' + A\overline{B}$
$S4 = \overline{A}BC' + AB$		$S4' = \overline{A}BD' + AB$

Where A is SSP signal, B is FPWM signal, C' is an APOD signal for cell 1 and D' is an APOD signal for cell 2. The MATLAB/ SIMULINK model for HMC is designed as subsystem and it is given in Fig. 6.

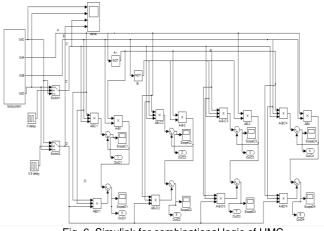


Fig. 6. Simulink for combinational logic of HMC

4 SIMULATION RESULTS

Cascaded five level inverter operation and its results at various load conditions are studied and discussed below. The block diagram of five level cascaded inverter with HAPOD scheme is shown in Fig. 7.

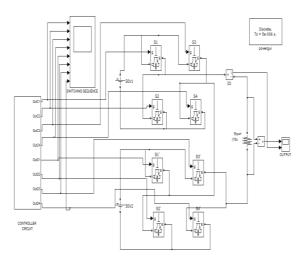


Fig. 7. Simulink for cascaded five level inverter

The switching sequence waveform of each switch S1 through S4 and S1' through s4' is shown in Fig. 8.



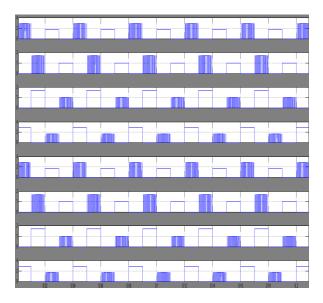
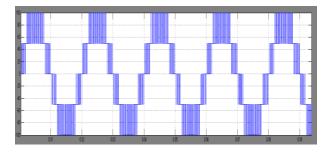


Fig. 8. Switching pulses

From the waveform we can observe that gate pulse of each switch has both FPWM and APOD signals. The input voltage applied is 50V and the load resistance is 10ohms, inductance 5mH, the corresponding output voltage and current of the proposed inverter is shown in Fig. 9.



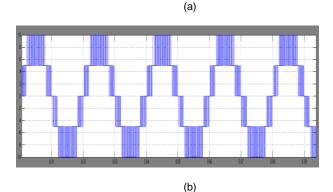
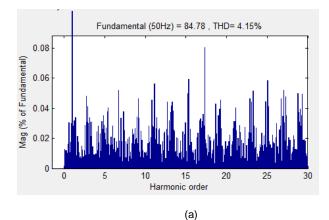
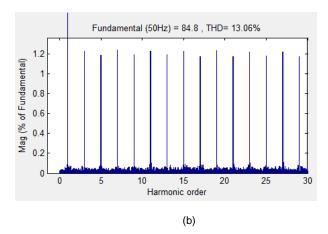


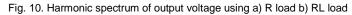
Fig. 9. (a) output voltage (b) output current

The total harmonic reduction THD for the output voltage using the R load is about 4.15% and for RL load it is about

13.52%. The Harmonic spectra of the output voltage waveform in the linear modulation region of (M=0.8) is shown in Fig. 10.







5 CONCLUSION

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In this paper, a sequential switching hybrid alternative phase opposition disposition technique for cascaded five level inverter is proposed. The output voltage and current waveforms are obtained for R and RL load. The Harmonic performance of this proposed scheme is analyed in the linear range of modulation index and it seems to be good. Hybrid modulations embedded with PWM circulation produces balanced power dissipation among the switches within the cell as well as series connected cells. This proposed modulation can be easily extended to higher voltage level.

REFERENCES

[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930-2945, Dec.2007.

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[4] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1047-1058, Mar. 2008.

[5] C. Govindaraju and K. Baskaran, "Efficient hybrid carrier based space vector modulation for cascaded multilevel inverter," J. Power Electron., vol. 10, no. 3, pp. 277–284, May 2010.

[6] S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching frequency modulation algorithm for high-power multilevel inverters," IEEE Trans.Ind. Electron., vol. 54, no. 5, pp. 2894-2901, Oct. 2007.

[7] Martha Calais, Lawrence J. Borlel Vassilios, G. Agelidis "Analysis of Multicarrier PWM Methods for a Single-phase Five Level Inverter", IEEE Transactions on Power Electronics, July 2001, pp 1351-1356.

[8] Zhou Jinghua and Li Zhengxi, -Research on Hybrid Modulation Strategies Based on General Hybrid Topology of Multilevel Inverter||, International symposium on Power Electronics Electrical Drives, Automation & Motion, IEEE Conf. Rec: 978-1-4244-1664-6, pp.784-788, 2008.

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